Remarks/Arguments

Reconsideration of this application is requested.

Extension of Time

A request for a one month extension of the period for response to the office action mailed on April 13, 2005 is enclosed. The extended period for response expires on August 15, 2005.

Claim Status

Claims 1-28 were presented. Claims 1, 9, 17, 18 and 23 are amended and claim 24 is canceled, without prejudice. Thus, claims 1-23 and 25-28 are now pending.

Allowable Subject Matter

The indication of allowable subject matter in claim 16 is noted and appreciated.

Claim Objections

Claims 9 and 18 are objected to because of grammatical informalities. In response, claims 9 and 18 are corrected as suggested in the Action.

Claim Rejections – 35 USC 112

Claims 1-13, 15, 17-22, 24 and 26-28 are rejected under 35 USC 112, second paragraph, as failing to comply with the enablement requirement. In response, applicant respectfully traverses the rejection and submits that the claims are fully enabled by the specification. The various issues raised in the Action are addressed below in the order as set forth in the Action.

1. The S/H Circuit and ADC Processing Unit Share a Single Op Amp

First, with respect to claim 1, the Action asserts that the sharing of a single operational amplifier between the sample-and-hold (S/H) circuit and the ADC processing unit is not described in sufficient detail to enable the invention. Applicant disagrees. Figure 5 depicts an algorithmic ADC comprising both a sample-and-hold circuit and an ADC processing unit. Figs. 7a-7j depict ten stages

of operation of the algorithmic ADC of Figure 5, as determined by the setting (i.e. opened or closed) of the various switches shown in Fig. 5.

Stages 2 and 3 (1B and 2A of the timing diagram of Fig. 1) depicted in Figs. 7b-7c are hold stages. As described in paragraphs [59]-[60], op amp 120 is utilized by the sample-and-hold portion of the ADC (i.e., capacitor C_s and its associated switches) during stages 2 and 3 to buffer the sampled input voltage held by capacitor C_s and charge capacitors $C_{\{0,1,2,3\}p}$ to the sampled voltage.

Stages 4-10 (2B-NB of the timing diagram of Fig. 1) depicted in Figs. 7d-7j are sampling and MDAC residue generation stages. As described in paragraphs [61]-[68], op amp 120 is disconnected from capacitor C_s during these stages. Instead, op amp 120 is utilized by the MDAC portion of the ADC (i.e. capacitors $C_{\{1,2,3\}p}$ and their associated switches) to generate residue voltages.

Thus, the specification and drawings clearly describe and enable a single operational amplifier (op amp 120) that is used by both a sample-and-hold circuit and an ADC processing unit. Accordingly, applicant traverses the rejection.

2. Parallel Operation of the S/H Circuit and ADC Processing Unit

Next, with respect to claim 1, the Action asserts that parallel operation of the ADC processing unit and the sample-and-hold (S/H) circuit and their sharing of a single operational amplifier is not described in sufficient detail to enable the invention. Applicant disagrees. The timing diagram of Figure 1 clearly shows that the sample-and-hold operation (S/H phases 18) is performed parallel in time with (i.e., at the same time as) the operation of the ADC processing unit (MDAC phases 14; sub-ADC phases 16). This parallel operation is described in detail throughout the specification and subsequent drawings. See, for example, Figs. 7g and 7h and paragraphs [65] and [66]. At the same time that sampling capacitor C_s samples the input analog signal (i.e., operation of the sample-and-hold circuit), MDAC 102 (capacitors $C_{\{1,2,3\}p}$ and op amp 120) proceeds with residue voltage generation (i.e., operation of the ADC processing unit).

For these reasons, applicant respectfully traverses the rejection. However, for clarification purposes, claim 1 is amended to recite that the sample-and-hold circuit and ADC processing unit operate *parallel in time.*

3. Known Algorithmic ADCs with a Common Op Amp

Next, the Action refers to applicant's statement in paragraph [04] that "known algorithmic ADCs comprise at least two single-bit processing units sharing a common operational amplifier", and asserts that since no further details are provided a comparison cannot be made with the inventions of claims 1, 15 and 24. On this point, the Examiner's attention is directed to the Nagaraj paper "Efficient Circuit Configurations for Algorithmic Analog to Digital Converters", which was disclosed by applicant in its IDS filed with the application on December 31, 2003. In Nagaraj's Figs. 5-7, an algorithmic ADC consisting of two processing units (unit 1: capacitors 1a and 2a; unit 2: capacitors 1b and 2b) that share a single op amp. The sample-and-hold operation is carried out by unit 1 (there is no dedicated S/H circuit), and it happens in series with the A/D conversion.

Applicant's S/H circuit, by contrast, uses an extra capacitor C_s and works in parallel with the A/D operation. As a result, applicant has the full length of the conversion cycle for S/H operation rather than just 1 Nth of it, which facilitates high speed operation.

4. Comparison to Pipelined ADCs

Next, the action references paragraph [38] and questions how applicant's invention is analogous to the process used in conventional pipelined ADCs. The exact language of the referenced portion of paragraph [38] is:

> After the N cycles, the N*K+1 bit analog-to-digital conversion result is formed using the sub-conversion results in a process analogous to the process used in pipelined analog-to-digital converters."

Thus, the only part that of applicant's invention that is "analogous" to pipelined ADC occurs after the inventive parallel operation of the S/H and ADC

units and use of a single op amp, when the final ADC output is formed using the partial results from each conversion step.

5. Parallel/Serial Operation

Next, the Action asks how the invention can follow a "heavily serial operation principle" (paragraph [36]) and also have units placed in a "parallel" configuration (paragraph [45]). As has been explained, the sample-and-hold operations are performed parallel in time with the ADC processing unit operations. The A/D conversion itself, however, is a serial operation. Thus, the serial A/D conversion operates in parallel with the sample-and-hold operation.

6. Integration and Parallel Operation of S/H Circuit and MDAC

Next, the Action asks how the S/H circuit can simultaneously be parallel to the MDAC and integrated with it. In response, reference is made to paragraph [78] of applicant's specification. Integration refers to the fact that the S/H circuit and the MDAC share the same op amp.

The Action refers to Figure 6 of Choi (US 5,952,952), which depicts an ADC stage 106 having an S/H circuit 240 and a DAC 220, and suggests that this corresponds to applicant's claimed integration of a S/H circuit and MDAC. Applicant disagrees. Choi's S/H circuit 240 is merely sampling and holding the residue voltage that is passed on to the next ADC stage. This function is also performed by applicant's MDAC circuit. However, applicant's claims are directed to a different S/H operation, sampling and holding the input analog signal to the algorithmic ADC itself, and an operation that is performed *in parallel* with the MDAC operation, and thus in parallel with the residue voltage sampling and holding performed by Choi's S/H circuit 240.

Applicant does not believe clarifying amendment to be necessary on this point, since the claims require operation of a sample-and-hold circuit *in parallel* with operation of an ADC processing unit. The referenced sample-and-hold circuit of Choi is part of the ADC processing unit, and thus cannot be in parallel with itself.

7. Intermediate Analog Voltage

Finally, the Action asserts that it is unclear what is meant by the term "intermediate analog voltage" in claim 17. In response, claim 17 is amended to recite a "new residue voltage" which is formed in part from "previous residue voltages", to correspond with the description in paragraph [41].

In view of applicant's explanations and amendments, where necessary, applicant submits that claims 1-13, 15, 17-22, 24 and 26-28 are fully enabled and that the rejections under 35 USC 112, first paragraph, should be withdrawn.

Claim Rejections -35 USC 103

Claim 14

Claim 14 is rejected under 35 USC 103(a) as obvious over the Admitted Prior Art (APA) in view of Choi. Applicant respectfully traverses the rejection. Claim 14 requires:

> ...sampling and holding the input analog signal during a sample-and-hold clock period...
>
> ...generating N sets of bits during the sample-and-hold clock period...

As discussed above with reference to known algorithmic ADCs, such as the ADC of the Nagaraj paper, the sample-and-hold operation is carried out in series with the A/D conversion (generating N sets of bits). Thus, APA does not disclose generating N sets of bits *during* the sample-and-hold period. That is, APA discloses generating N sets of bits *after* the sample-and-hold period.

Choi does not cure the deficiencies of APA. Like APA, Choi discloses generation of N bits (i.e. stages 106A, 106B, 106C) only *after* an analog input 102 is provided (thus, after the input 102 has been sampled and held). Hence, Choi does not teach or suggest generating the N bits during the sample-and-hold period and does not cure the deficiencies of APA.

For these reasons, the rejection of claim 14 under 35 USC 103(a) should be withdrawn.

Claims 23 and 25

Claims 23 and 25 are rejected under 35 USC 103(a) as obvious over APA in view of Brooks et al. (US 5,847,600). In response, claim 23 is amended to include the limitations of claim 24, which requires that:

> the means for sampling and holding an input signal, means for applying the sampled and held signal to a switched capacitor circuit, and means for generating a residue voltage comprise a single operational amplifier

As has been discussed, the use of a single operational amplifier for both sample-and-hold operations and ADC processing operation is not disclosed by the art of record. The rejections of claims 23 and 25 under 35 USC 103(a) should be withdrawn.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The Action asserts that various claimed features are not shown in the drawings. In response, applicant submits that its responses to the claim rejections under 35 USC 112, first paragraph, also clarify and serve to overcome the drawing objections. In particular:

The parallel operation of the ADC processing unit and S/H circuit is shown in at least Fig. 1 and Figs. 7a-7j.

Integration of the S/H circuit and MDAC (sharing a single operational amplifier) is shown at least in Figs. 5 and 7a-7j.

A sample-and-hold circuit is shown at least in Figs. 5 and 7a-j.

Conclusion

This application is now believed to be in condition for allowance. The Examiner is invited to telephone the undersigned to resolve any issues that remain after entry of this amendment.

Any fees due with this response may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

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By: _____

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